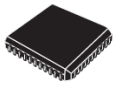
L6451

28 channel inkjet driver

Features

- Multipower BCD technology
- 40 V DMOS output breakdown
- Precise output energy
- ESD output protection with clamping diodes
- Very low quiescent current
- PLCC44 package



PLCC44

Description

The L6451 is realized in Multipower BCD Technology which combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same IC. By using mixed technology it has been possible to optimize the logic circuitry and the power stage to achieve the best possible performances.

Intended to be used in inkjet printer applications as a 4 to 28 (2 x 14) line selectable decoder/driver, the L6451 device driver has the advantages of low power CMOS inputs and logic, with 28 high current and high voltage DMOS outputs capable of sustaining a maximum of 40 V.

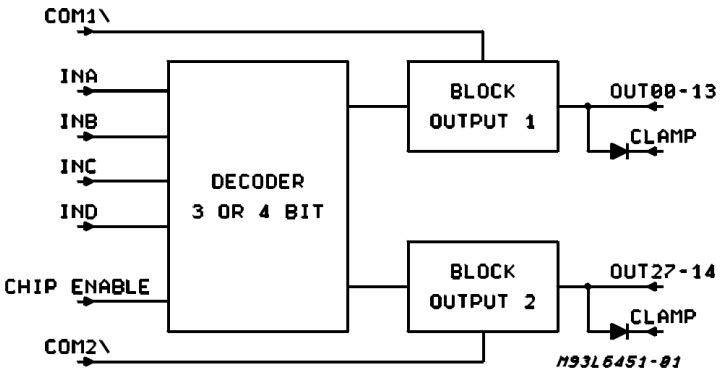
On system power up the output drivers are locked out using the chip enable function; two enable inputs are available for the different driver banks. An internal power-on system is implemented in order to avoid wrong output commutation during the supply voltage transients.

Using a mask option during manufacturing allows a different decoding. Control of the energy delivered to the print head is made by means of a special circuitry. All driver outputs are capable of withstanding a contact discharge of +/-8 kV with the IC biased.

Table 1. Device summary

Order codes	Package
L6451	PLCC44
L6451013TR	PLCC44 in tape and reel
L6451DIE8	DIE

Figure 1. Block diagram (4-bit case)



1 Pin information

Figure 2. Pin connection (top view)

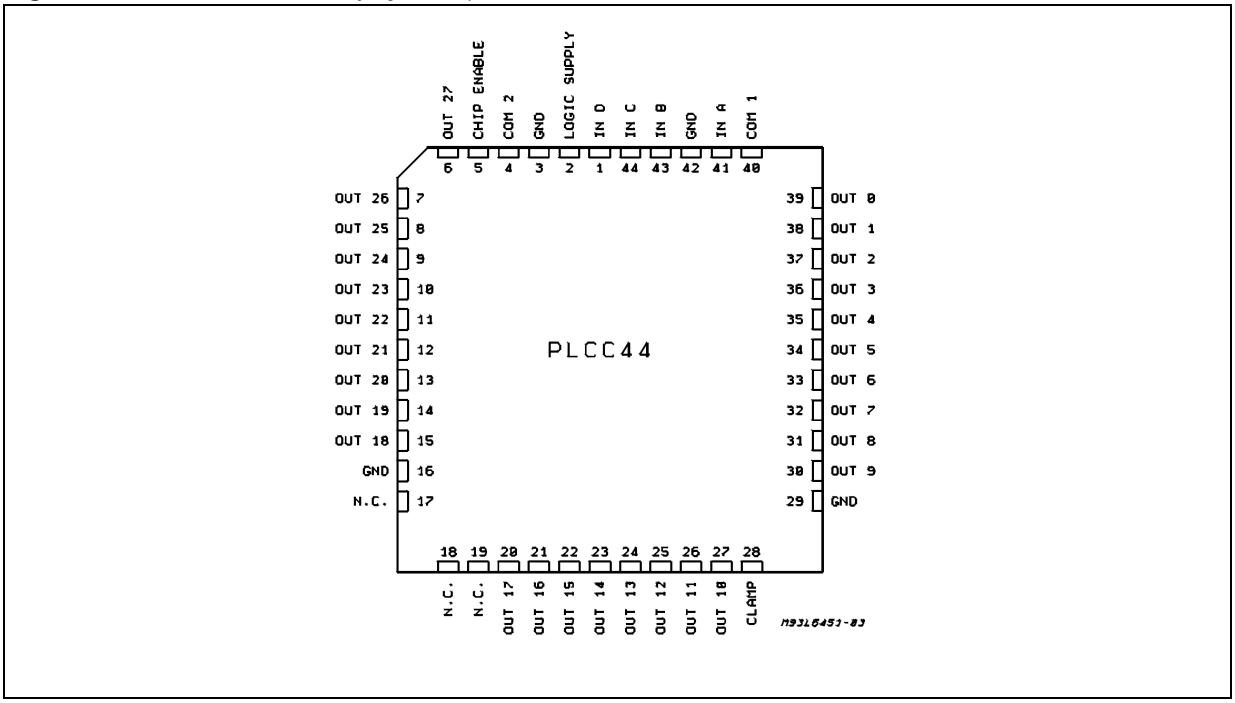


Table 2. Pin description

Pin Name	Function
V_{DD}	5 V logic supply.
GND	Logic and power ground.
OUT0 to OUT27	DMOS outputs.
CLAMP	This pin has to be connected to the power supply voltage of the head resistors. Each of the output DMOS have their drain connected with the anode of a protection diode, all the cathodes of the protection diodes are connected to the clamp pin. In order to have the device supplied, the CLAMP pin needs to be connected to the power.
INA, INB, INC, IND	Decoder inputs.
COM1, COM2	A low logic input on these pins enables the outputs selected by the decoder inputs.
CHIP ENABLE	A logic high enable the chip.

2 Electrical characteristics

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{OUT}	Output voltage	40	V
V_{CLAMP}	Output clamping voltage	40	V
I_{OUT}	Output continuous current	0.8	A
I_{PEAK}	Output peak current (with duty cycle = 10% TON= 4 ms)	2	A
T_J	Junction temperature	150	°C
V_{DD}	Logic supply voltage	7	V
V_{IN}	Input voltage range	-0.3 V to V_S+0.3	V
T_{amb}	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature range	-55 to 150	°C

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient max.	65(1)	°C/W

1. Device mounted on PCB.

Table 5. DC electrical characteristcs(1)

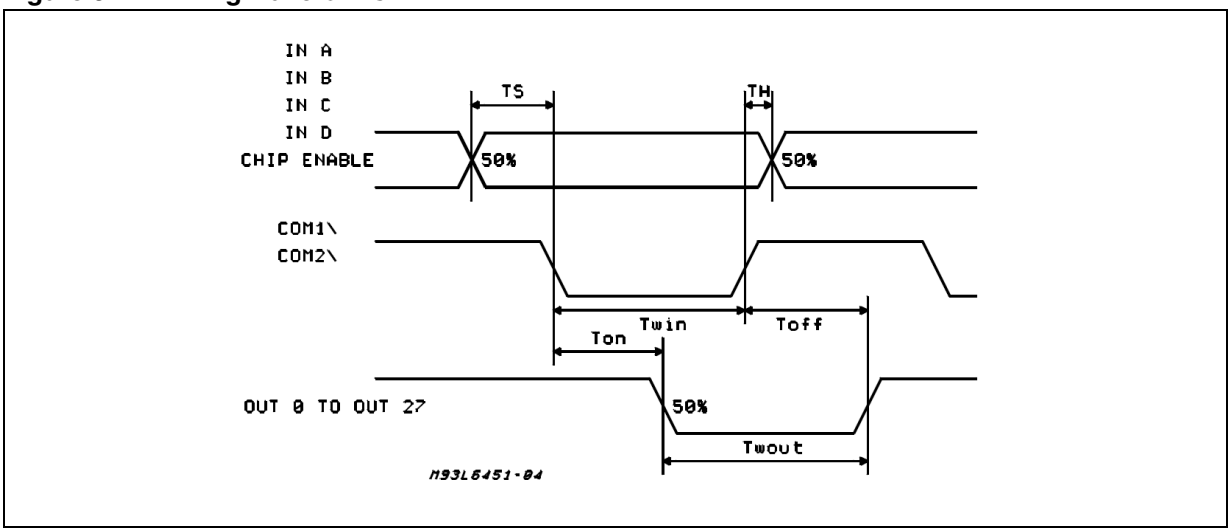
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Logic supply voltage		4.75	5	5.25	V
V_{CLAMP}	Clamping voltage		9		38	V
V_{IL}	Low level input voltage				1.2	V
V_{IH}	High level input current		V_{DD} -1.2			V
I_{LL}	Low level input current	$V_{IN}= V_{IL}$			-200	µA
I_{LH}	High level input current	$V_{IN}= V_{IH}$			10	µA
I_{DD}	Logic supply current	(Independent from the output conditions)			5	mA
V_{OUT}	Output saturation voltage	Tj = 25 °C D.C. 0.4 A		0.9		V
		Tj = 25 °C D.C. 0.5 A		1.1		V
		Tj = 90 °C D.C. 0.4 A		1.4		V
		Tj = 90 °C D.C. 0.5 A		1.7		V
ΔV_{CE}	Output saturation absolute voltage variation around the typ. values for extended temperature ranges	Tj = 25° C to 90° C D.C.: 0.4 A Tj = 25° C to 90° C D.C.: 0.5 A			±0.2 ±0.25	V V
$R_{DS}ON$				2.2		Ω

1. T_{amb} = 25°C, V_{DD} = 5V, V_{clamp} = 18 V unless otherwise specified

Table 6. AC electrical characteristics

Symbol	Signal Name	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T_S	INA, INB, INC, IND Vs COMn	SET - UP time		30			ns
T_H	INA, INB, INC, IND Vs COMn	HOLD time		0			ns
T_{on}	COM1,2,3,4 V_S OUT 0 to N	TURN - ON time	I_{OUT}= 0.5 A, R_L= 39 Ω T_j= 25 to 90 °C		150		ns
T_{off}	COM1,2,3,4 V_S OUT 0 to N	TURN - OFF time	I_{OUT}= 0.5 A, R_L= 39 Ω T_j= 25 to 90°C		150		ns
t_r		Rise time			100		ns
t_f		Fall time			100		ns
T_{wout}		Output pulse width	T_{win}= 3.5 ms R_L= 40 Ω I_{OUT}= 0.5 A	-20	T_{win}	+80	ns
ΔP_D		Maximum allowable variation of the output power transmitted by each driver to the resistive load	R_L= 39 Ω V_{CLAMP}= 18 V			±4	%
			R_L= 40 Ω V_{clamp}= 18 V		±4		%

Figure 3. Timing waveforms

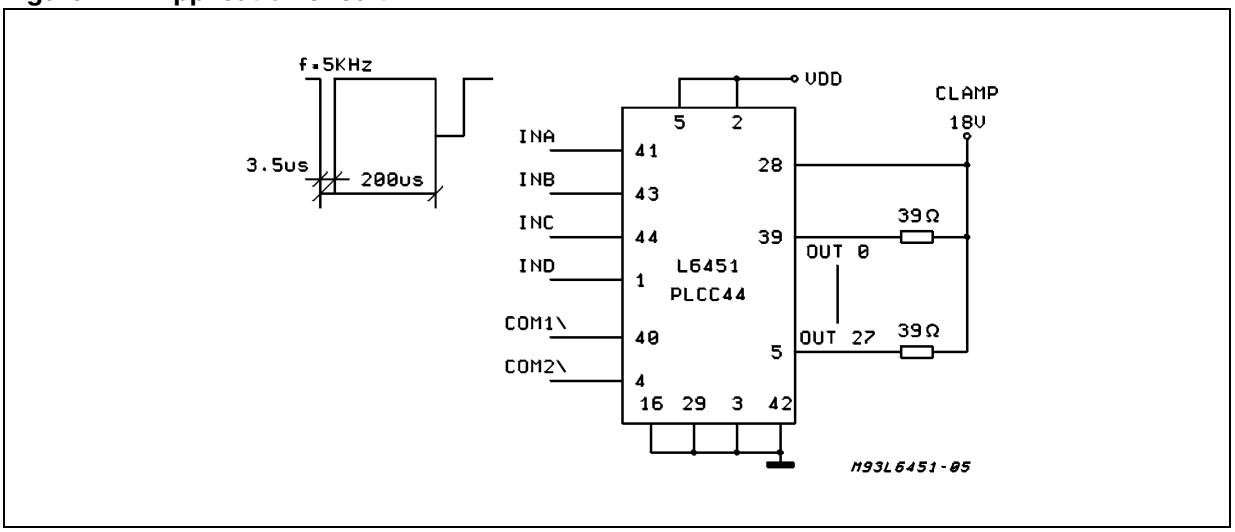


3 Functional description

Table 7. Decoder truth table

IND	INC	INB	INA (LSB)	OUTPUTS
0	0	0	0	0.27
0	0	0	1	1.26
0	0	1	0	2.25
0	0	1	1	3.24
0	1	0	0	4.23
0	1	0	1	5.22
0	1	1	0	6.21
0	1	1	1	7.20
1	0	0	0	8.19
1	0	0	1	9.18
1	0	1	0	10.17
1	0	1	1	11.16
1	1	0	0	12.15
1	1	0	1	13.14
1	1	1	0	ALL OFF
1	1	1	1	ALL OFF

Figure 4. Application circuit



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
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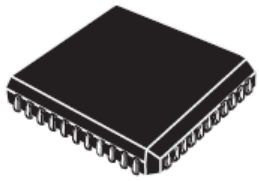
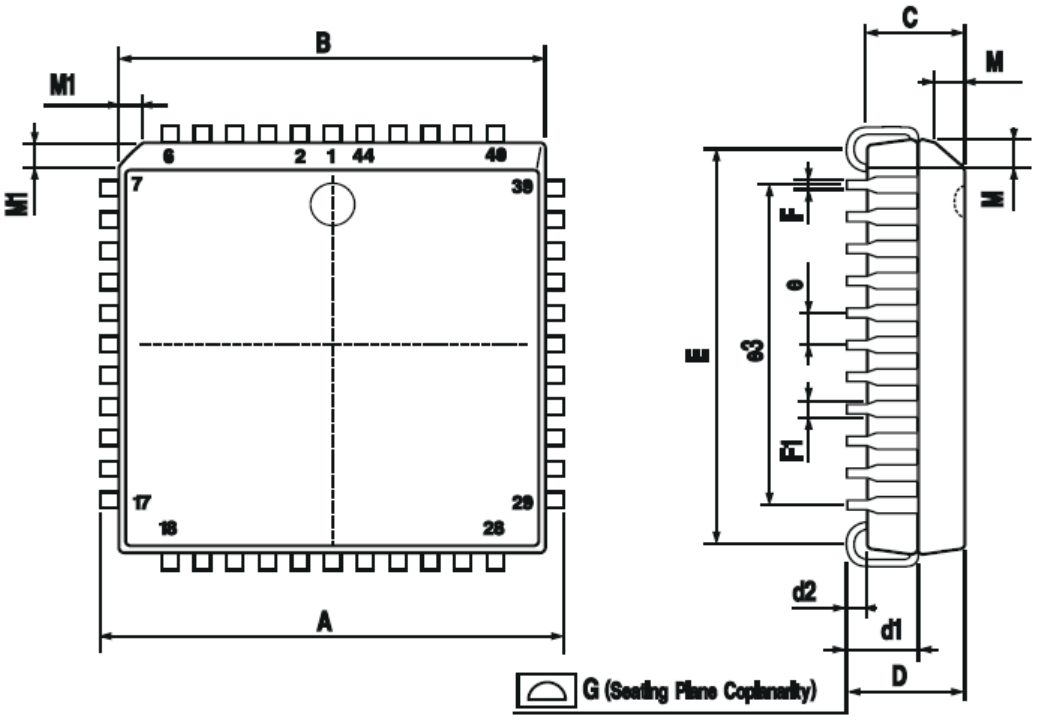
Figure 5. PLCC44 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

OUTLINE AND MECHANICAL DATA



PLCC44



Revision history

Table 8. Document revision history

Date	Revision	Description of Changes
Dec-2000	2	First Issue in EDOCS dms
May -2005	3	Changed only look and feel layout
02-Apr-2009	4	Converted to corporate template. Added ECOPACK information.

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